



## **PATENT**



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re:

Horiuchi et al.

Serial No.:

09/812,276

Filed:

March 20, 2001

Title:

SEMICONDUCTOR DEVICE

AND PROCESS OF PRODUCTION

OF SAME

Examiner:

Patricia M. Costanzo

Atty Doc. No. 72-01

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Post Office as first class mail postage prepaid in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20221 on July

29, 2002

nn F. McNulty, Reg. No. 3,028 Dated: July 29, 2002

Commissioner of Patents Washington, DC 20231

## **COVER LETTER WITH CERTIFICATE OF MAILING**

Sir:

Enclose please find the following documents:

- (1) Cover Letter with Certificate of Mailing;
- (2) Amendment (3 pages);
- (3) Abstract Of The Disclosure (1 page);
- (4) Clean Copy of Specification Pages 5, 7, and 38;
- (5) Clean Copy of Claim 21; and
- (6) Paul & Paul Postcard to be returned by the PTO.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES ASSOCIATED WITH THIS COMMUNICATION, OR CREDIT ANY OVERPAYMENT, TO PAUL & PAUL DEPOSIT ACCOUNT NO. 16-0750, ORDER NO. <u>0-745</u>.

Respectfully submitted.

ohn F. McNulty, Esquire

Registration No. 23,028

Paul & Paul

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ECHNOLOGY CENTER ? POT

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Amendment

Sir:

This is in response to the Official Action of May 2, 2002.

Please amend the above-identified application as follows:

Please replace the Abstract Of The Disclosure with the enclosed replacement sheet comprising an Abstract Of The Disclosure with 150 words or fewer.

Please amend the specification as follows:

Page 5, line 5 after "layer and", insert -- forming throughholes in the thickness direction--

A2

Page 7, line 19 after "arranged" insert -- in --.

Page 38, line 15, change "129" to -- 124 --.

NE

Replacement pages for pages 5, 7 and 38 are provided herewith.

In the claims:

Re-write claims 21 as follows:

A3

21. (Amended) A semiconductor device as set forth in claim 20, wherein the top surface of said <u>resin member</u> [sealing resin layer] and the back surface of said semiconductor element form substantially the same plane.